**In the Claims**

Please replace claims 99, 105, 106, 107, 108, 109, and 112 with the following clean version of the amended claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i). Cancel all previous versions of any amended claim.

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii). Any claim not accompanied by a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

99. (amended) A semiconductor transistor structure comprising:

a region of a semiconductor wafer;

a gate over the region, the gate having first and second sidewalls;

first conductivity type heavily doped first and second source/drain regions proximate the first and second sidewalls, respectively;

first and second oxide layers extending along and at least partially covering the first and second sidewalls, respectively;

B3

first and second sidewall spacers extending along and at least partially covering the first and second oxide layers, respectively, the entirety of the semiconductor wafer under the first and second sidewall spacers being defined as first and second segments, respectively, and the first and second segments being separated from respective first and second source/drain regions by respective first and second gap regions, no part of the first and second gap regions being under respective first and second sidewall spacers; and

second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments.



B

7 105. (amended) A semiconductor transistor device comprising:

a transistor gate over a semiconductor material wafer, the transistor gate having opposing first and second sidewalls;

first conductivity type, heavily doped, first and second opposing source/drain regions within the semiconductor material wafer beside respective first and second sidewalls;

first and second opposing oxide layers extending along and covering the respective first and second sidewalls;

B4 first and second opposing sidewall spacers extending along and at least partially covering respective first and second oxide layers;

first and second opposing segments consisting of an entirety of the semiconductor wafer material under respective first and second sidewall spacers, the first and second opposing segments being separated from the first and second opposing source/drain regions by respective first and second gap regions of the semiconductor material wafer;

second conductivity type, first and second opposing halo regions within the respective first and second gap regions and not extending into respective first and second segments; and

one of the first and second conductivity types being n-type and the other of the first and second conductivity types being p-type.



B

8 7

~~106~~. (amended) The device of claim ~~105~~ wherein the first and second opposing halo regions extend directly under a full lateral extent of the respective first and second source/drain regions.

9 7

~~107~~. (amended) The device of claim ~~105~~ wherein the first and second gap regions each have a lateral length of from about 150 to about 600 Angstroms.

Cont'd B4

10 7

~~108~~. (amended) The device of claim ~~105~~ wherein the first and second oxide layers extend laterally out from the respective first and second sidewalls, directly under the respective first and second sidewall spacers, and directly over respective first and second segments.

11 10

~~109~~. (amended) The device of claim ~~108~~ wherein the first and second oxide layers further extend past the respective first and second sidewall spacers, directly over the respective first and second gap regions, and directly over at least a portion of respective first and second source/drain regions.

19

112. (amended) A semiconductor transistor structure comprising:

a region of a semiconductor wafer;

a gate over the region, the gate having first and second opposing sidewalls;

first conductivity type heavily doped first and second opposing source/drain regions proximate the first and second opposing sidewalls, respectively;

B5

first and second opposing oxide layers extending along and at least partially covering the first and second sidewalls, respectively;

first and second sidewall opposing spacers extending along and at least partially covering the first and second opposing oxide layers, respectively, the entirety of the semiconductor wafer under the first and second opposing sidewall spacers being defined as first and second segments, respectively, and the first and second segments being separated from respective first and second source/drain regions by respective first and second gap regions, no part of the first and second gap regions being under respective first and second sidewall spacers; and

second conductivity type halo regions within the first and second gap regions and not extending into the first and second segments, wherein one of the first and second conductivity types is n-type and the other is p-type.



B